Non-Blocking Switching Fabric Bandwidth - Official Technical Overview & Hardware Datasheet

EXECUTIVE SUMMARY

The relentless growth of hyperscale cloud computing, 5G backhaul, and AI-driven data aggregation demands a fundamental shift in switching architecture. Traditional shared bus and blocking fabrics introduce unpredictable latency and throughput bottlenecks under microburst traffic conditions. The non-blocking switching fabric bandwidth architecture eliminates these constraints by providing full-rate, simultaneous communication between all ingress and egress ports.

This document details the technical specifications, hardware implementation, and performance guarantees of our seventh-generation Crossbar + Shared Memory hybrid fabric. Capable of delivering line-rate, lossless switching up to 51.2 Tbps in a single chassis, this architecture ensures that any port can communicate with any other port at wire speed without contention.

ARCHITECTURE & CHASSIS DESIGN

The non-blocking fabric is realized through a distributed, three-stage Clos architecture implemented on redundant fabric cards. Each line card hosts a local switching element (LSE) that interfaces with a central fabric element (CFE).

Key architectural tenets:

- Work-conserving arbitration: A modified iSLIP scheduler achieves 100% throughput under uniform and non-uniform traffic patterns.

- VOQ (Virtual Output Queue) buffering per egress port, preventing Head-of-Line (HOL) blocking.

- Cell-based switching: Ingress packets are disassembled into fixed-size 80-byte cells for deterministic scheduling, then reassembled at egress.

- Cut-through forwarding mode supported for latency-sensitive applications

(sub-400ns port-to-port).

HARDWARE FEATURES

1. FABRIC REDUNDANCY: N+1 fabric card redundancy with hitless failover (< 50 ms switchover).

2. BUFFER ARCHITECTURE: 64 GB shared buffer pool (dynamic per-port allocation).

3. FLOW CONTROL: 802.3x Pause and Priority Flow Control (PFC, 802.1Qbb).

4. TELEMETRY: In-band Network Telemetry (INT) capable fabric monitors per-hop latency and queue depth.

5. POWER EFFICIENCY: 0.35 Watts per Gbps under full load, adaptive voltage scaling.

COMPLIANCE & STANDARDS

- IEEE 802.3ae (10GE), 802.3ba (40/100GE), 802.3ck (400GE)

- CE, FCC Part 15 Class A, VCCI, RCM

- RoHS, REACH, WEEE

- GR-1089-CORE (EMC), GR-63-CORE (NEBS Level 3)

TECHNICAL SPECIFICATIONS

Switching Fabric: Distributed non-blocking, cell-based Clos

Bandwidth per Slot: 3.2 Tbps (full-duplex)

Aggregate System Bandwidth: Up to 51.2 Tbps

Forwarding Rate: 10.2 Bpps (billion packets per second)

Latency (store-and-forward): < 1.2 µs (64-byte frame)

Jitter: < 30 ns (deterministic scheduling)

MTBF: 1,250,000 hours (fabric card)

Parameter	**Specification**
Form Factor	12RU Centralized Chassis or 7RU Distributed Spine
Switching Capacity	51.2 Tbps (full-duplex, non-blocking)
Power Supply	3+3 Redundant, Hot-swappable AC (200-240V) or DC (-48V)
Fabric Card Slots	6 (N+1 redundancy active standard)
Per-Slot Bandwidth	3.2 Tbps bidirectional
Operating Temperature	0 °C to 45 °C (derated above 1800m altitude)
Max Power Consumption	2850W (fully loaded line cards & fabric)

ORDERING OPTIONS

Base Chassis SKU: NBS-7K-48-SLOT (48 line card slots)

Fabric Card SKUs:

- NBS-FAB-S3 (3.2 Tbps, base)

- NBS-FAB-S6 (6.4 Tbps, high-capacity)

- NBS-FAB-R (Redundant, hot-swappable)

Line Card Compatibility: All NBS-7K series line cards (1GE to 400GE interfaces).

Optional Accessories:

- Front-to-rear airflow kit

- AC/DC power shelf (3+3 or N+1)

- Fabric extension cable set (inter-chassis linking)