Policy-Based Routing PBR Hardware Support - Official Technical Overview & Hardware Datasheet

POLICY-BASED ROUTING PBR HARDWARE SUPPORT: OFFICIAL TECHNICAL OVERVIEW & HARDWARE DATASHEET

EXECUTIVE SUMMARY

Leveraging granular traffic steering capabilities directly at the forwarding plane, the Policy-Based Routing (PBR) hardware support architecture delivers deterministic, application-aware path selection without reliance on traditional routing table lookups. This datasheet documents the complete hardware-level implementation of PBR across the carrier-grade router portfolio, including ASIC-level classification engines, line-rate filtering resources, and redundant policy enforcement mechanisms. All PBR operations are executed in hardware to ensure zero performance penalty relative to conventional destination-based forwarding.

ARCHITECTURE & CHASSIS DESIGN

The PBR-capable hardware platform is organized around a centralized crossbar switching fabric with distributed forwarding engines. Each line card integrates a Ternary Content-Addressable Memory (TCAM) co-processor dedicated to policy matching, supporting up to 16,000 unique classification entries per slot. The system backplane operates at 1.2 Tbps per slot (full-duplex) to accommodate simultaneous policy-based redirection, mirroring, and next-hop override operations. Chassis options range from compact 1RU edge units to 21-spline modular core systems, with PBR feature parity maintained across all form factors.

HARDWARE FEATURES

ASIC-Level PBR Classification: The custom Forwarding Engine ASIC (FEA-9th Gen) evaluates Layer 3 and Layer 4 headers against user-defined policies before consulting the FIB. Match criteria include source/destination IP prefixes, protocol type, DSCP/ToS values, TCP/UDP port ranges, and input interface.

Line-Rate Performance: All PBR actions — including set next-hop, set output interface, set QoS group, and policy-based discard — execute at wire speed. No architectural rate limiting is imposed on classified traffic flows.

Resilient Policy Storage: PBR policy tables are mirrored across redundant routing engine (RE) modules. In case of active RE failover, policies are reinstalled on all line cards within sub-second timeframes (<500 ms).

High-Availability Integration: When paired with Bidirectional Forwarding Detection (BFD), PBR hardware can trigger next-hop failover within 50 ms upon neighbor loss, independent of routing protocol convergence.

COMPLIANCE & STANDARDS

This hardware implementation adheres to: RFC 1812 (Requirements for IP Version 4 Routers) PBR extensions; IETF IPPM framework for performance measurement; NEBS Level 3 (GR-63-CORE, GR-1089-CORE); ETSI EN 300 386;

RoHS 2011/65/EU.

TECHNICAL SPECIFICATIONS

Parameter	Specification
Form Factor	1RU / 2RU / 4RU modular chassis options
Switching Capacity	Up to 12.8 Tbps (non-blocking, full-duplex)
Power Supply	1+1, 2+2 redundant AC (110-240V) / DC (-48V)
TCAM Entries (PBR)	4,000 standard / 16,000 max per slot
Maximum PBR Policies	10,000 (system-wide, hardware-resident)
Forwarding Rate (IPv4/IPv6)	2.4 Bpps (billions of packets per second)
BFD Echo Mode Latency	< 1 ms (hardware timestamped)
Operating Temperature	0°C to 55°C (NEBS: -5°C to 55°C)
MTBF (calculated)	312,000 hours (Telcordia SR-332)

ORDERING OPTIONS

Base SKU: RTR-7200-PBR (1RU chassis, integrated PBR license, 2x10GE management ports). Line Card PBR Expansion Licenses: LC-PBR-2K (2,000 additional TCAM entries), LC-PBR-8K (8,000 additional entries). Redundant Fabric Modules: FAB-7200-R (required for stateful PBR failover). Field-upgradeable accessory kit for optical bypass: BYP-OPT-40G. All SKUs include three-year hardware warranty with lifetime PBR firmware updates.