Systems Engineering Technical Reference Manual: How to Limit Bandwidth Per Port on Switch

SYSTEMS ENGINEERING TECHNICAL REFERENCE MANUAL: HOW TO LIMIT BANDWIDTH PER PORT ON SWITCH

PRODUCT IDENTIFICATION

Document Identifier: SERM-BPS-2026-001

Product Series: OmniFabric BPS (Bandwidth Policy Switch) Series

Hardware Revision: 4.0 and later

Firmware Baseline: OSN 12.6 or higher

The OmniFabric BPS product family delivers carrier-grade, per-port bandwidth control as a native hardware feature, eliminating software-induced latency and jitter. This document specifies the architectural implementation, configuration parameters, and performance guarantees for ingress/egress rate-limiting on a per-interface basis.

SYSTEM HARDWARE TOPOLOGY

The BPS series implements bandwidth limiting at the physical layer (PHY) and data link layer (MAC) using a distributed forwarding ASIC architecture. Each front-panel port is serviced by a dedicated Hardware Policer Engine (HPE-800) capable of:

- Dual-rate token bucket algorithm (CIR / EIR)
- Peak Information Rate (PIR) enforcement with 1 Kbps granularity
- Burst size definition from 1 KB to 128 MB

Supported Port Types for Direct Rate Limiting:

- 10/100/1000BASE-T (RJ45) – port groups GbE-24
- 1000BASE-X / 10GBASE-R (SFP/SFP+) – port groups SFP+-12
- 25GBASE-R / 100GBASE-R (QSFP28) – port groups Q28-4

DATA & CONTROL PLANE CAPABILITIES

Control Plane Integration:

- CLI (Network Operating System shell)

- SNMP MIB-1213 Rate Limit Objects

- RESTCONF / NETCONF with native OpenConfig model: openconfig-qos-elements

- gNMI telemetry for real-time policer statistics

Data Plane Enforcement Modes:

- Egress shaping (per-queue + per-port)

- Ingress policing (color-aware / color-blind)

- Storm control (broadcast, multicast, unknown unicast)

- Adaptive rate limiting based on queue depth (optional AI-RL mode)

COMPONENT BREAKDOWN – PER-PORT BANDWIDTH LIMITER

1. Hardware Token Bucket Engine (per port): 4 dynamic buckets (CIR, PIR, CBS, PBS)

2. Dedicated Bandwidth Profile Memory: 8 profiles per port, up to 2000 system-wide

3. Queuing architecture: 8 hardware queues per port (strict priority + DWRR)

4. Timestamp resolution for rate correction: 8 ns

5. Measurement interval: configurable from 1 ms to 1 s

OPERATIONAL SPECS MATRIX

Minimum guaranteed granularity: 1 Kbps (1000 bps) for all port speeds

Maximum per-port rate limit value: line rate of the physical interface (e.g., 10 Gbps on SFP+ port)

Burst tolerance deviation: < 0.05% from configured value at 64-byte frames

Latency introduced by policer: < 640 ns (in cut-through mode)

Parameter	**Specification**
Form Factor	1RU / 2RU Chassis (BPS-4824 / BPS-4896 respectively)
Per-Port Granularity	1 Kbps minimum increment across all port speeds
Switching Capacity (non-blocking)	Full fabric: up to 2.56 Tbps (BPS-4896)
Power Supply	1+1 Hot-swappable AC (100-240V) or DC (-48V)
Supported Ports per System	24x GbE RJ45 + 12x 10G SFP+ (BPS-4824) | 96x 10G SFP+ (BPS-4896)

Concurrent Rate Limit Profiles	Up to 2000 system-wide, 8 per port
Measured Policing Accuracy	± 0.05% deviation at 64-byte frame size

REGULATORY COMPLIANCE

Rate limiting functionality complies with:

- MEF 10.3 (Bandwidth Profile for EVC)

- IEEE 802.1Qav (Credit-Based Shaper for AVB)

- ITU-T Y.1564 (Policing accuracy test methodology)

- RFC 4115 (Differentiated Service Two-Rate, Three-Color Marker)

Safety and EMC: UL 60950-1, FCC Part 15 Class A, CE, EN55032, AS/NZS CISPR32

DEPLOYMENT COMPLIANCE STATEMENT: This device supports in-service bandwidth modification without link flap or traffic disruption. Configuration changes to policer rates are applied within one scheduler cycle (max 10 ms).