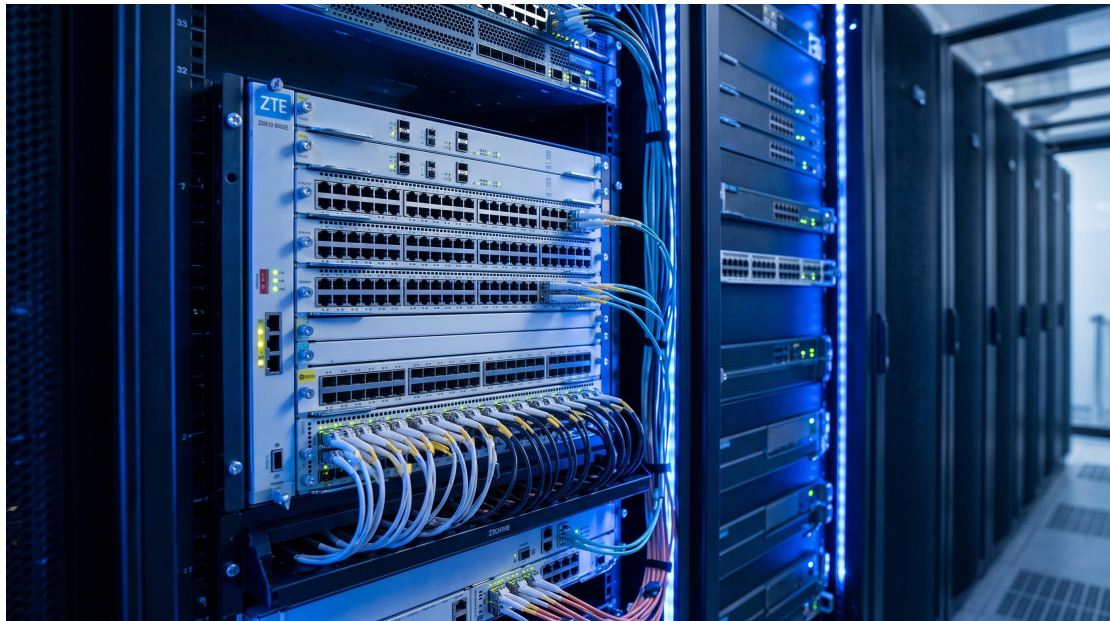


Systems Engineering Technical Reference Manual: ZTE ZXR10 8900E Core Switch Line Card MAC Address Table Limits

PRODUCT IDENTIFICATION

The ZXR10 8900E Series represents ZTE's flagship carrier-grade core switching platform, engineered for the rigorous demands of metropolitan area networks, large-scale campus backbones, and high-density enterprise data center cores. The platform is purpose-built to deliver non-blocking, wire-speed forwarding across a scalable architecture supporting up to 10.24 Tbps system switching capacity and up to 1.28 Tbps per slot.

This Systems Engineering Technical Reference Manual addresses the MAC address table limits and associated Layer 2 forwarding table management capabilities of the ZXR10 8900E line cards. It provides network architects and systems engineers with authoritative specifications for planning, deploying, and optimizing MAC address table utilization within carrier-grade environments.



SYSTEM HARDWARE TOPOLOGY

The ZXR10 8900E employs a modular, distributed switching architecture in which each service line card operates as an autonomous forwarding entity. Unlike centralized architectures, every line card maintains its own forwarding table, enabling wire-speed local forwarding decisions and eliminating the need to traverse the switch fabric for intra-card traffic.

The platform supports a comprehensive line card portfolio spanning Fast Ethernet, Gigabit Ethernet, 10 Gigabit Ethernet, 40 Gigabit Ethernet, and 100 Gigabit Ethernet interfaces. High-capacity line cards include 48-port wire-speed 10GE, 8-port 40GE, and 4-port 100GE configurations, enabling granular scalability from 10GE to 100GE deployments.

The system backplane utilizes a passive, large-capacity high-speed design employing 10G SerDes connections between main control switching cards and line cards. This architecture reserves substantial bandwidth headroom for future upgrades to 400G platforms and 100G line cards.

DATA & CONTROL PLANE CAPABILITIES

MAC Address Table Architecture

The ZXR10 8900E line cards implement a comprehensive MAC address management subsystem that serves as the fundamental forwarding table for Layer 2 Ethernet switching. Each line card maintains a local forwarding table synchronized with the system-wide MAC address database.

The platform supports a system-level MAC table depth of 512K entries, providing substantial capacity for large-scale enterprise and carrier deployments. This MAC address capacity is coupled with 4M RIB entries, 512K forwarding route entries, and 256K ACL entries, positioning the 8900E for the most demanding network environments.

MAC Address Learning and Synchronization

MAC address learning operates in accordance with IEEE 802.1D bridging standards, with dynamic learning enabled on a per-port basis. The system maintains MAC address synchronization across all line cards and main control modules to ensure consistent forwarding decisions throughout the chassis.

Aging mechanisms are configurable per VLAN and per port, with default aging times optimized for typical enterprise traffic patterns. The system supports both dynamic aging and static MAC entry preservation to accommodate environments requiring persistent address mappings.

MAC Address Management Functions

The ZXR10 8900E provides a comprehensive suite of MAC address management capabilities:

MAC Address Binding: Enables administrators to bind specific MAC addresses to designated switch ports, disabling dynamic learning for bound addresses. This function restricts user physical location and protects critical MAC addresses from spoofing or unauthorized relocation.

MAC Address Filtering: Provides source and destination MAC-based packet filtering, enabling the switch to discard packets to or from specific MAC

addresses. This capability supports access control policies and undesired user isolation.

MAC Address Number Limit: Allows administrators to limit the number of MAC addresses learned on specific ports, preventing system resource exhaustion during denial-of-service attacks and controlling user density per port.

MAC Address Freeze: Enables freezing of MAC address entries on stable physical ports, such as uplink interfaces, preventing network disconnection caused by infringement of critical MAC addresses.

MAC Address Multi-Angle Display: Provides display and statistical analysis of VLAN tables by VLAN, port, and static/dynamic classification, facilitating network diagnosis and operational monitoring.

COMPONENT BREAKDOWN

The MAC address table functionality of the ZXR10 8900E is implemented across multiple hardware components:

Forwarding ASIC: Each line card houses a custom forwarding ASIC that performs hardware-based packet parsing, classification, and forwarding

decisions. The ASIC maintains the local MAC address forwarding table and executes lookup operations at wire speed, ensuring line-rate performance regardless of table occupancy.

Packet Buffer Pool: Each line card is equipped with up to 128 MB of distributed packet buffer memory. The buffering architecture employs dynamic queue management supporting Weighted Random Early Detection and tail drop policies, providing fine-grained Quality of Service control for MAC address-based traffic classification.

Main Control Module: The main control switching card maintains the system-wide MAC address database and orchestrates synchronization across all line cards. The module is deployed in 1:1 and 1+1 redundancy configurations to ensure uninterrupted MAC address management services.

Backplane Interconnect: The passive optical backplane provides high-bandwidth serial links operating at 25 Gbps and 50 Gbps per lane, aggregating to support the total system switching capacity. MAC address synchronization traffic traverses these links between line cards and control modules.

OPERATIONAL SPECS MATRIX

The following table provides a consolidated reference for MAC address table limits and related Layer 2 forwarding parameters of the ZXR10 8900E Series.

Parameter	Specification
System MAC Table Depth	512K entries (system-wide)
Forwarding Route Entries	512K
RIB Entries	4M
ACL Entries	256K
MAC Address Learning Scope	Per line card local forwarding table with system-wide synchronization
MAC Address Aging	Configurable per VLAN and per port; dynamic aging supported
MAC Address Binding	Supported; disables dynamic learning for bound addresses
MAC Address Filtering	Supported; source and destination MAC-based filtering
MAC Address Number Limit	Configurable per port; prevents resource exhaustion
MAC Address Freeze	Supported; prevents address table modification on designated ports
MAC Address Display	Multi-angle display by VLAN, port,

	static/dynamic classification
Line Card Forwarding	Wire-speed local forwarding decisions per line card
Buffer Capacity per Line Card	Up to 128 MB distributed packet buffer

REGULATORY COMPLIANCE

The ZXR10 8900E Series complies with applicable international standards for Ethernet switching and carrier-grade telecommunications equipment. Key compliance areas relevant to MAC address table functionality include:

IEEE 802.1D MAC Bridges: Defines the fundamental bridging and MAC address learning behavior implemented by the platform.

IEEE 802.1Q VLAN Tagging: Specifies VLAN-aware MAC address table partitioning, enabling independent MAC address learning domains per VLAN.

IEEE 802.1ad Provider Bridging: Extends VLAN and MAC address table scaling for carrier Ethernet deployments requiring QinQ encapsulation.

IEEE 802.1X Port-Based Network Access Control: Integrates with MAC address authentication to enforce port security policies.

IEEE 802.3az Energy Efficient Ethernet: Optimizes power consumption based on traffic patterns, including idle periods when MAC address table activity is minimal.

